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A LOW POWER CMOS LC VCO IN 70NM FOR RF APPLICATIONS

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ABSTRACT

This paper proposes a low power cross coupled differential LC Voltage Controlled Oscillator topology which has been designed using 70nm CMOS process for wireless applications. To achieve low power, NMOS cross-coupled differential LC VCO topology is used. In this topology a variable MOS capacitance has been used to obtain high frequency tuning range by varying gate voltage of MOS in order to meet this VCO topology for RF applications. Simulation result is performed by Tanner EDA 14.0 on 70nm CMOS process. The tuning frequency of circuit is from 5.05 to 5.37 GHz that can obtain by applying tuning voltage ranging from 0.1 to 1 V. The proposed VCO topology dissipates power of 0.4mw at the maximum oscillation frequency which is very low compared to conventional VCO.

KEYWORDS: Voltage, Controlled Oscillator (VCO), CMOS, NMOS, Tuning Rang and RF

INTRODUCTION

Oscillators are integral part of many electronic systems which is ranges from clock generation in microprocessor to carrier synthesis in cellular telephones requiring vastly different oscillator topologies and performance parameter. Recently the explosive growth in the field of wireless communication and the advances in complementary metal oxide semiconductor (CMOS) technology have made it possible to implement high frequency oscillator with CMOS technology. The oscillators are required to be tunable over a relatively wide frequency range. The tunability is usually obtained by variable voltage and hence comes the name Voltage Controlled Oscillator (VCO). VCO is the key component in frequency synthesizer for Radio Frequency (RF) wireless application. Voltage Controlled Oscillators constitute a critical component in many RF transceivers and are commonly associated with signal processing tasks like frequency selection and signal generation. Now days, RF transceivers require programmable carrier frequencies, and rely on phase locked loops (PLLs) to accomplish the same. These PLLs embed a less accurate RF oscillator in a feedback loop whose frequency can be controlled with a control signal [1-2].

The key metrics of a VCO are phase noise at certain range of frequency, tuning range of the frequency, power consumption and area. All these key metrics trade with each others. The selection of VCO for an application depends on these key metrics. The ring VCO and LC VCO topologies have to meet all the key metrics. The VCO for wireless application require outstanding phase noise performance and low power consumption. In LC VCO, the phase difference between tank voltage and tank current is zero i.e. LC VCO has inherent filtering action which substantially reduces phase noise. Due to this reason LC VCO is preferred over the ring VCO for wireless applications [3].

There are different topologies for designing, LC tank VCO which have been cited in [4-6]. They are One-transistor Oscillator Topology, Cross-coupled differential topology, CMOS core cross-coupled differential topology, Quadrature VCO with reconfigurable LC tank VCO. One transistor topology has larger transistor area compared to cross coupled differential topology. For this reason cross coupled differential topology is considered more suitable topology than one transistor topology, for fully integrated CMOS VCO. CMOS Core cross coupled topology exhibits higher parasitic

capacitance over cross coupled differential topology. Increasing the parasitic capacitance means lowering the tuning range. For this reason CMOS cross coupled topology is not prefer for high frequency wireless applications [7-13]. In [14] a switched capacitor array, two power supply and substrate noise filter are involved in the CMOS cross coupled topology. This proposes a wide band LC VCO which can be used for low phase noise and low power consumption applications.

The Quadrature VCO with reconfigurable LC tank topology is used by Cheol-Hoe Kim et.al [15] to obtain wide band tuning range for wireless application. This topology consumed more power for high frequency operation so it needs to be more optimized. In [16-19] cross coupled differential topology proposed for low power, low phase noise and low frequency operation. This topology has low transistor area compared to all there topologies.

This paper proposes a cross coupled differential topology for low power consumption and high frequency application. The objective of proposed design is to achieve high frequency operation and low power consumption at 70nm CMOS process without involving switched capacitor array and two power supply.

Rest of the paper is organized as follows, in section II; basic feedback model for oscillator & Barkhausen criteria is discussed. The proposed cross coupled differential topology & simulation result are discussed in section III. Simulation results are compared in section IV, whereas section V concludes the paper.

FEEDBACK MODEL OF OSCILLATOR

A simple oscillator produces a periodic output usually in the form of voltage. Oscillators are nonlinear in nature, though are usually viewed as a linear time invariant feedback system as shown in Figure 1. In the *s*-domain, the transfer function of this negative feedback system is given by

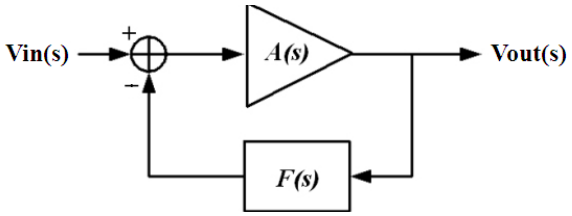

Figure 1: Negative Feedback System with Frequency Selective Network

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1+A(s)F} \quad (1)$$

This system provides a periodic output at frequency $S=j\omega_0$.If the loop gain A(s) F(s) is equal to -1 at a specific frequency ω_0, the closed loop gain approach to infinity. Under this condition the circuit amplifies its own noise component indefinitely and system trends to be unstable. In summary, if a negative feedback circuit has a loop gain that satisfies two conditions:

$$|A(j\omega_0)F(j\omega_0)| \geq \quad (2)$$

$$\angle |A(j\omega_0)F(j\omega_0)| = 1 \quad (3)$$

The Barkhausen Criteria for oscillation is necessary but not sufficient [1].

CROSS-COUPLED DIFFERENTIAL TOPOLOGY

The cross coupled differential topology has parallel combination of lossy LC tank section, crossed coupled NMOS transistor pair, variable capacitor and current mirror as shown in figure 2. LC tank section has inductor (L), capacitor(C) and parallel LC tank resistance (R_p). Cross coupled MOS transistor pair provides an equivalent negative

resistance is used to compensate LC tank equivalent parallel resistance. A PMOS cross-coupled transistor pair has been adopted in a VCO design for claiming low noise characteristics of a PMOS device itself. The hot carrier effect is found to be small in a PMOS. This is a critical condition in a CMOS process where hot electron noise is significant. Flicker noise of a PMOS is approximate ~10 times smaller than that of a NMOS for the same transistor dimension. Considering that a PMOS transistor has a lower mobility, the flicker noise of a PMOS should be lower at a given current and g_m as larger gate area. For these reasons, it has been reported that a VCO using a cross-coupled PMOS pair shows low phase noise characteristics. PMOS devices have to be twice the size of NMOS devices to achieve similar transconductance parameters. Due this reason NMOS cross coupled pair transistor is more preferred over PMOS cross coupled pair transistor in this topology [16-18].

In order to achieve a desirable control over the negative resistance and evidently, the oscillation amplitude, a current mirror is generally adopted to limit the supply current. The bias current that flows through current mirror is referred to as the tail current and sets the total power dissipation. However, in some cases, it has been reported that it may be advantageous to entirely eliminate the tail current source to achieve better phase noise characteristics [6].

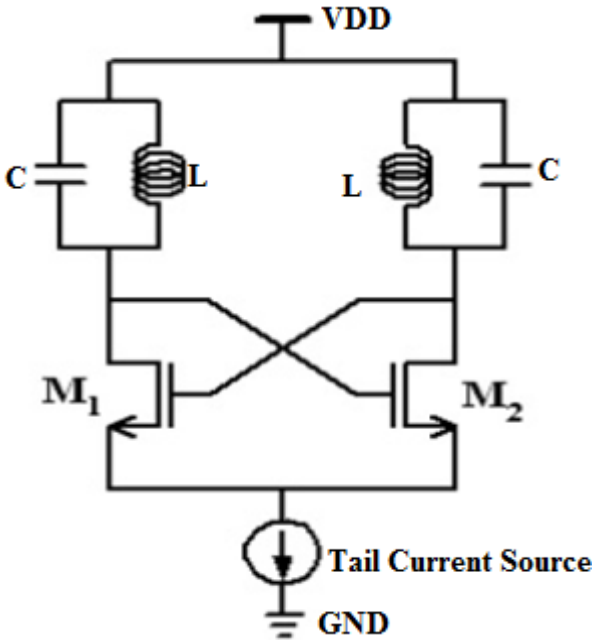

Figure 2: Cross Coupled Differential Topology

VCO DESIGN

Negative Resistance

In Differential cross coupled VCO topology, the loss associated with LC tank circuit is given by the one-port model of oscillator as show in figure 3 [19]. They are associated as:

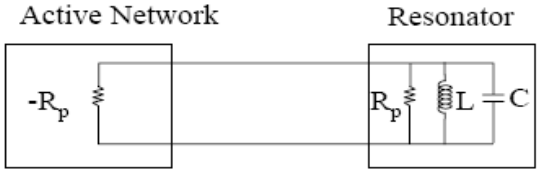

Figure 3: One Port Model of Cross Coupled Differential Topology

The resonator LC tank has parasitic resistances (R_p) which prevent the resonator from oscillation because the stored energy will leak through the resistance. To compensate this loss, negative parallel resistances ($-R_p$) can be added to the resonator so that the energy loss in R_p is replenished by the negative resistance. The negative resistance's

implementation is typically by an active network [4-5]. The equivalent parallel negative tank resistance is inversely proportional to transconductance of tank is given below:

$$G_{tank} = \frac{1}{R_p} \tag{4}$$

Therefore, in order to ensure oscillations, and to compensate the tank losses, negative transconductance associated with the active device (NMOS) pairs M_1 and M_2 is G_m and negative (R_{in}) of cross coupled pair transistor are given by relation given below:

$$R_{in} = -\frac{2}{G_m} \tag{5}$$

The transconductance of NMOS pair G_m should be greater than and equal to transconductance of LC tank G_{tank} in order to get sustain oscillation from VCO. The relation between G_m and G_{tank} is given by:

$$G_m \geq G_{tank} \tag{6}$$

MOS Varactor

The MOS capacitor has a structure that is analogous to a parallel plate capacitor with the drain, source and bulk (D, S, and B). In this proposed topology a PMOS transistor connected together realizing one plate of the capacitor, while the polysilicon gate constituting the other. The capacitance of such a structure shows non-linear dependence on the gate-bulk voltage V_{BG} [9] [19]. The resulting MOS capacitor is illustrated in Figure 4.

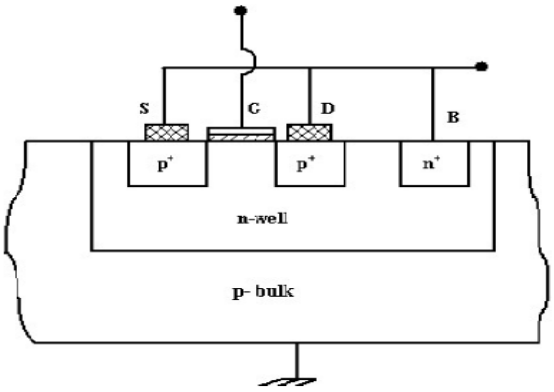

Figure 4: MOS Capacitor

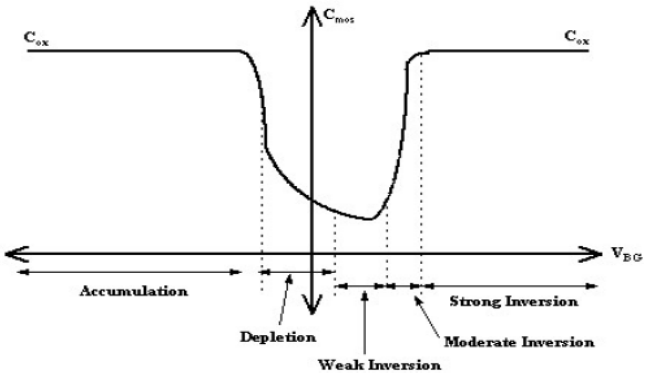

Figure 5: Capacitance versus Voltage Characteristics of a MOS Capacitor

Final Proposed VCO Design

The circuit schematic of the proposed LC VCO is shown in Figure 6. The topology of proposed VCO is based on NMOS cross-coupled differential LC structure (N-pair) with NMOS tail current source. This structure, once optimized,

performs better than other common VCO topologies, in terms of the power consumption and high frequency of operation for RF application.

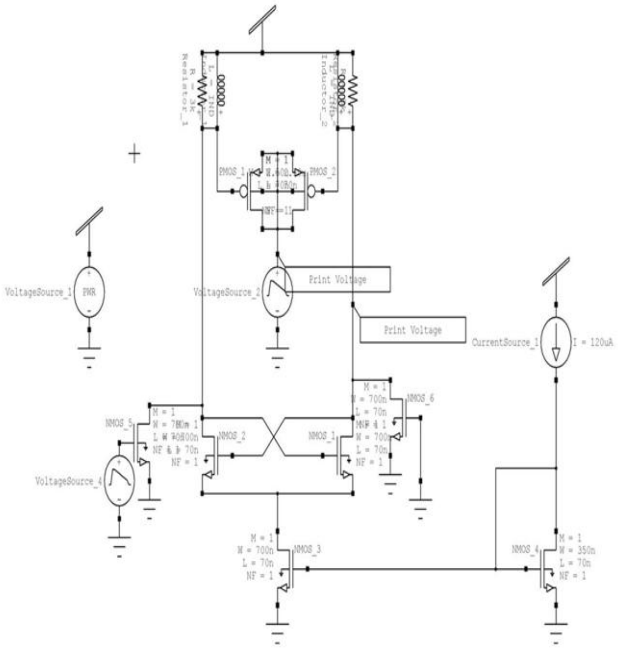

Figure 6: Proposed Crossed Coupled Differential LC VCO Topology

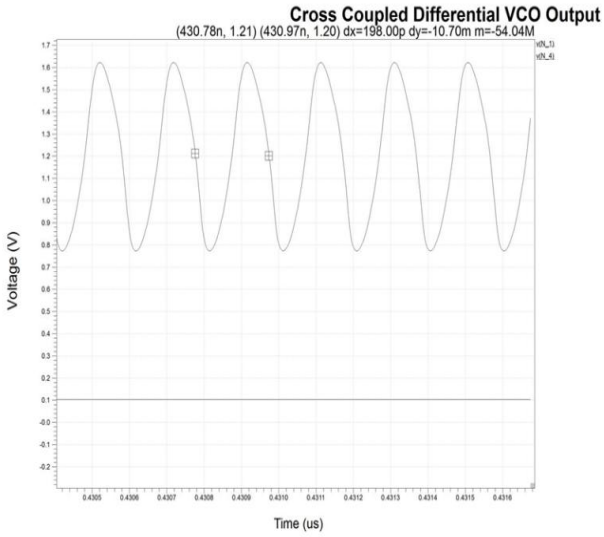

Figure 7: Simulation Result of Proposed Crossed Coupled Differential LC VCO Topology

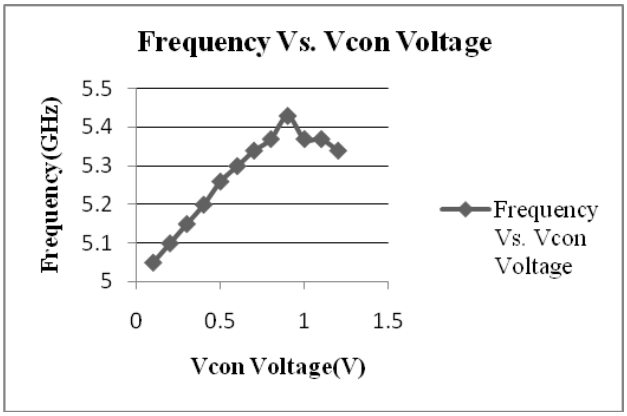

Figure 8: Frequency vs. v_{con} Voltage Plot

COMPARISON AND DISCUSSION

A comparison of this work with previous wide-tuning range design is shown in Table I. From this comparison table, it is seen that cross coupled differential LC VCO topology has low power consumption and high frequency for RF application.

Table 1: Comparison of Parameter

Mode	This Work	Ref.14
Technology	70nm	65nm
Frequency(in GHz)	5.05-5.37	0.75-1.5
Power Consumption	0.4mW	3.4mW
Tuning Range	6.14%	83%
Tuning Voltage	0.1-1V	--

CONCLUSIONS

A low power high frequency cross coupled differential LC VCO topology is realized in the Tanner 14.0 on 70nm CMOS technology for RF applications. The tuning Frequency range of the VCO is from 5.05 to 5.37 GHz with tuning voltage from 0.1 to 1 V while consuming 0.4mw power. The primary advantage of this topology is low-power consumption and high frequency operation for wireless applications.

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